TelCom Semiconductor, Inc.

TCM809
TCM810

3-PIN µP RESET MONITORS

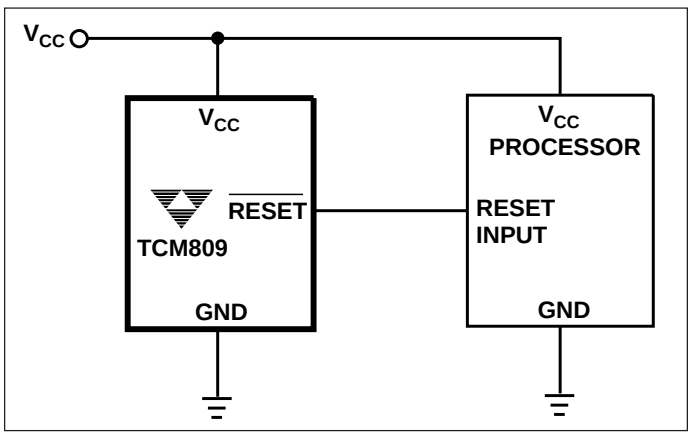
FEATURES

- **Precision V_{CC} Monitor for 3.0V, 3.3V, 5.0V Nominal System V Supplies**
- **140msec Guaranteed Minimum $\overline{\text{RESET}}$, RESET Output Duration**
- **$\overline{\text{RESET}}$ Output Guaranteed to V_{CC} = 1.0V (TCM809)**
- **Low 17µA Supply Current**
- **V_{CC} Transient Immunity**
- **Small SOT-23B-3 Package**
- **No External Components**

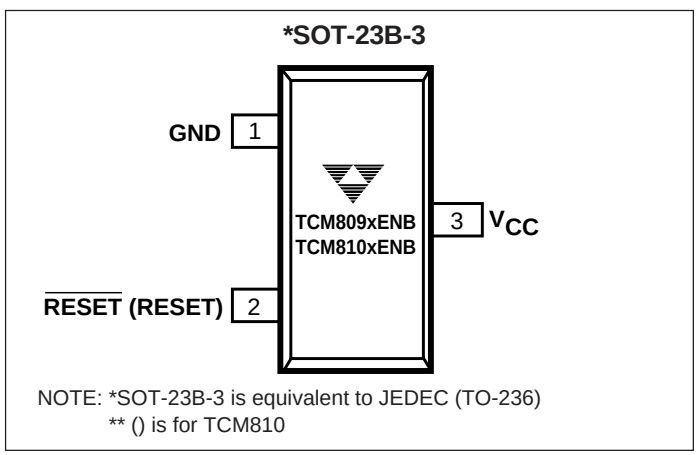
TYPICAL APPLICATIONS

- **Computers**
- **Embedded Systems**
- **Battery Powered Equipment**
- **Critical µP Power Supply Monitoring**

TYPICAL OPERATING CIRCUIT



PIN CONFIGURATION



NOTE: *SOT-23B-3 is equivalent to JEDEC (TO-236)
** () is for TCM810

GENERAL DESCRIPTION

The TCM809 and TCM810 are cost-effective system supervisor circuits designed to monitor V_{CC} in digital systems and provide a reset signal to the host processor when necessary. No external components are required.

The reset output is driven active within 20msec of V_{CC} falling through the reset voltage threshold. Reset is maintained active for a minimum of 140msec after V_{CC} rises above the reset threshold. The TCM810 has an active-high reset output while the TCM809 has an active-low reset output. The output of the TCM809 is guaranteed valid down to V_{CC} = 1V. Both devices are available in a SOT-23B-3 package.

The TCM809/810 are optimized to reject fast transient glitches on the V_{CC} line. Low supply current of 17µA (V_{CC} = 3.3V) makes these devices suitable for battery powered applications.

ORDERING INFORMATION

Part No.	Package	Temp. Range
TCM809xENB	SOT-23B-3	– 40°C to +85°C
TCM810xENB	SOT-23B-3	– 40°C to +85°C

NOTE: The "X" denotes a suffix for V_{CC} threshold - see table below.

Suffix	Reset V_{CC} Threshold (V)
L	4.63
M	4.38
T	3.08
S	2.93
R	2.63

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ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{CC} to GND) ..... +6.0V
$\overline{RESET}$, RESET ..... – 0.3V to (V_{CC} + 0.3V)
Input Current, V_{CC}.. ..... 20mA
Output Current, $\overline{RESET}$, RESET 20mA
dV/dt (V_{CC}) 100V/μS
Operating Temperature Range ..... – 40°C to +85°C
Power Dissipation ($T_A \leq 70°C$)
SOT-23B-3 (derate 4mW/°C above +70°C) ... 230mW
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +260°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_{cc} = 5V, T_A = Operating Temperature Range unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
	V_{CC} Range	T_A = 0°C to +70°C	1.0	—	5.5	V
		T_A = – 40°C to +85°C	1.2	—	5.5	
I_{CC}	Supply Current	TCM8xxL/M: V_{CC} < 5.5V	—	24	60	μA
		TCM8xxR/S/T: V_{CC} < 3.6V	—	17	50	
V_{TH}	Reset Threshold	(Note 2)				
		TCM8xxL: T_A = +25°C	4.56	4.63	4.70	V
		T_A = – 40°C to +85°C	4.50	—	4.75	
		TCM8xxM: T_A = +25°C	4.31	4.38	4.45	
		T_A = – 40°C to +85°C	4.25	—	4.50	
		TCM8xxT: T_A = +25°C	3.04	3.08	3.11	
		T_A = – 40°C to +85°C	3.00	—	3.15	
		TCM8xxS: T_A = +25°C	2.89	2.93	2.96	
		T_A = – 40°C to +85°C	2.85	—	3.00	
		TCM8xxR: T_A = +25°C	2.59	2.63	2.66	
		T_A = – 40°C to +85°C	2.55	—	2.70	
	Reset Threshold Tempco		—	30	—	ppm/°C
	V_{CC} to Reset Delay	(Note 2)				
		V_{CC} = V_{TH} to (V_{TH} – 100mV)	—	20	—	μsec
	Reset Active Timeout Period		140	240	560	msec
V_{OL}	$\overline{RESET}$ Output Voltage Low (TCM809)	TCM809R/S/T: V_{CC} = V_{TH} min, I_{SINK} = 1.2mA	—	—	0.3	V
		TCM809L/M: V_{CC} = V_{TH} min, I_{SINK} = 3.2mA	—	—	0.4	
		V_{CC} > 1.0V, I_{SINK} = 50μA	—	—	0.3	
V_{OH}	$\overline{RESET}$ Output Voltage High (TCM809)	TCM809R/S/T: V_{CC} > V_{TH} max, I_{SOURCE} = 500μA	0.8 V_{CC}	—	—	V
		TCM809L/M: V_{CC} > V_{TH} max, I_{SOURCE} = 800μA	V_{CC} – 1.5	—	—	
V_{OL}	RESET Output Voltage Low (TCM810)	TCM810R/S/T: V_{CC} = V_{TH} max, I_{SINK} = 1.2mA	—	—	0.3	V
		TCM810L/M: V_{CC} = V_{TH} max, I_{SINK} = 3.2mA	—	—	0.4	
V_{OH}	RESET Output Voltage High (TCM810)	1.8 < V_{CC} < VTH min, I_{SOURCE} = 150μA	0.8 V_{CC}	—	—	V

NOTES: 1. Production testing done at T_A = +25°C, over temperature limits guaranteed by design.
2. $\overline{RESET}$ output for TCM809, RESET Output for TCM810.

PIN DESCRIPTION

Pin No. (SOT-23B-3)	Symbol	Description
1	GND	Ground
2	$\overline{RESET}$ (TCM809)	$\overline{RESET}$ output remains low while V_{CC} is below the reset voltage threshold, and for 240msec (140msec min.) after V_{CC} rises above reset threshold.
2	RESET (TCM810)	RESET output remains high while V_{CC} is below the reset voltage threshold, and for 240msec (140msec min.) after V_{CC} rises above reset threshold.
3	V_{CC}	Supply voltage (Typ. +3.0V to +5.0V)

APPLICATIONS INFORMATION

V_{CC} Transient Rejection

The TCM809/810 provides accurate V_{CC} monitoring and reset timing during power-up, power-down, and brownout/sag conditions, and rejects negative-going transients (glitches) on the power supply line. Figure 1 shows the maximum transient duration vs. maximum negative excursion (overdrive) for glitch rejection. Any combination of duration and overdrive which lies **under** the curve will **not** generate a reset signal. Combinations above the curve are detected as a brownout or power-down. Transient immunity can be improved by adding a capacitor in close proximity to the V_{CC} pin of the TCM809/810.

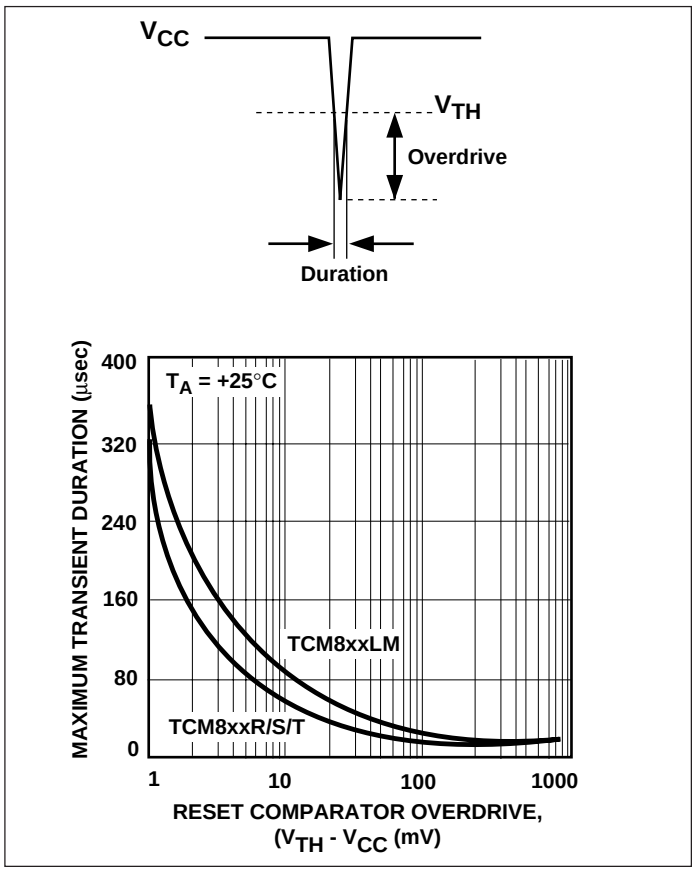

Figure 1. Maximum Transient Duration vs. Overdrive for Glitch Rejection at 25°C

$\overline{\text{RESET}}$ Signal Integrity During Power-Down

The TCM809 $\overline{\text{RESET}}$ output is valid to V_{CC} = 1.0V. Below this voltage the output becomes an "open circuit" and does not sink current. This means CMOS logic inputs to the μP will be floating at an undetermined voltage. Most digital systems are completely shutdown well above this voltage. However, in situations where $\overline{\text{RESET}}$ must be maintained valid to V_{CC} = 0V, a pull-down resistor must be connected from $\overline{\text{RESET}}$ to ground to discharge stray capacitances and hold the output low (Figure 2). This resistor value, though not critical, should be chosen such that it does not appreciably load $\overline{\text{RESET}}$ under normal operation (100kΩ will be suitable for most applications). Similarly, a pull-up resistor to V_{CC} is required for the TCM810 to ensure a valid high $\overline{\text{RESET}}$ for V_{CC} below 1.0V.

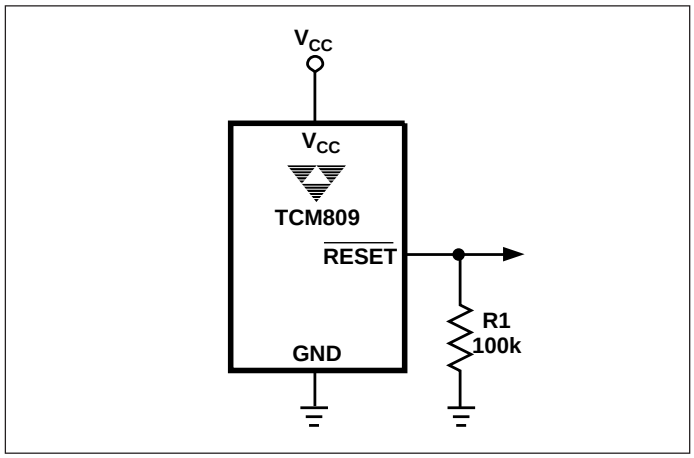

Figure 2. Ensuring RESET Valid to V_{CC} = 0V

Processors With Bidirectional I/O Pins

Some μP's (such as Motorola 68HC11) have bidirectional reset pins. Depending on the current drive capability of the processor pin, an indeterminate logic level may result if there is a logic conflict. This can be avoided by adding a 4.7k resistor in series with the output of the TCM809/810 (Figure 3). If there are other components in the system which require a reset signal, they should be buffered so as not to load the reset line. If the other components are required to follow the reset I/O of the μP, the buffer should be connected as shown with the solid line.

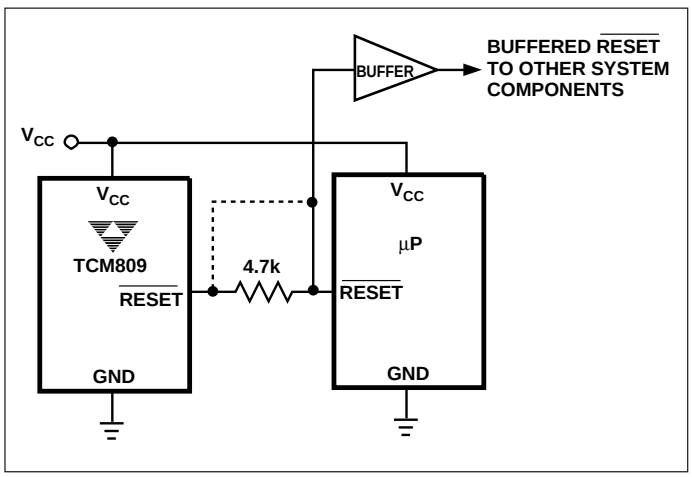

Figure 3. Interfacing to Bidirectional Reset I/O

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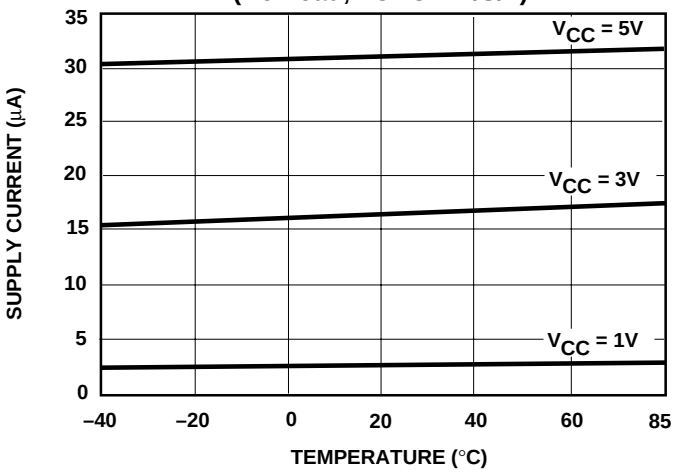
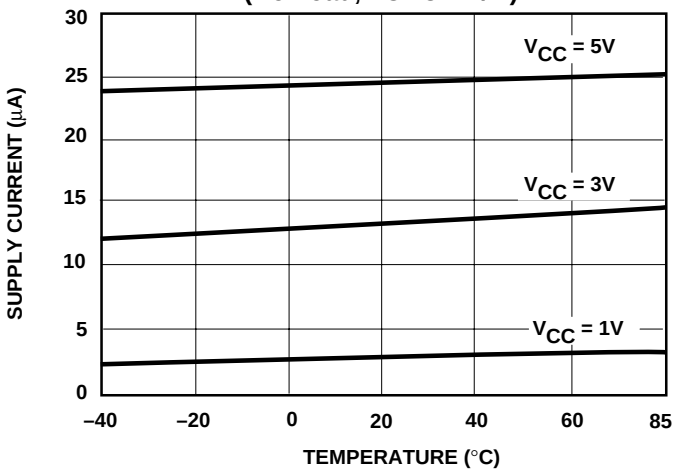
TYPICAL CHARACTERISTICS

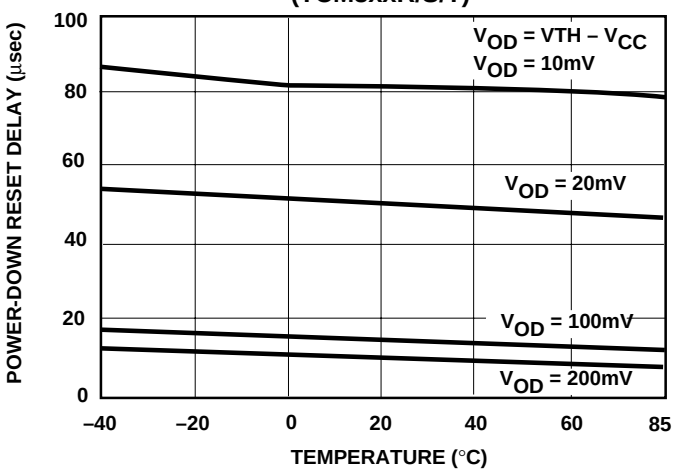
Supply Current vs.Temperature (No Load, TCM8xxR/S/T)



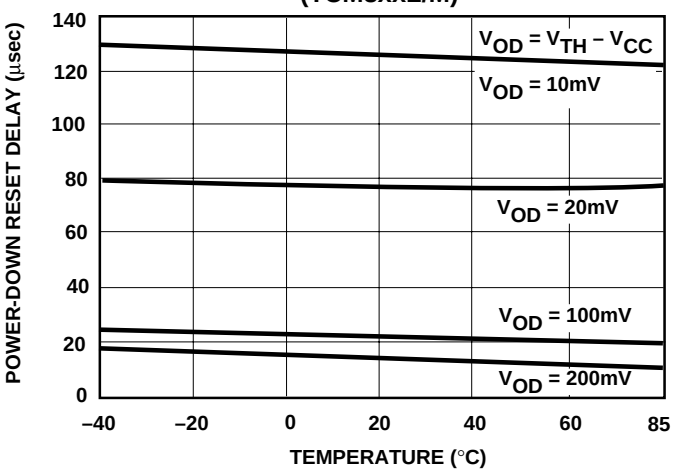
Supply Current vs.Temperature (No Load, TCM8xxL/M)



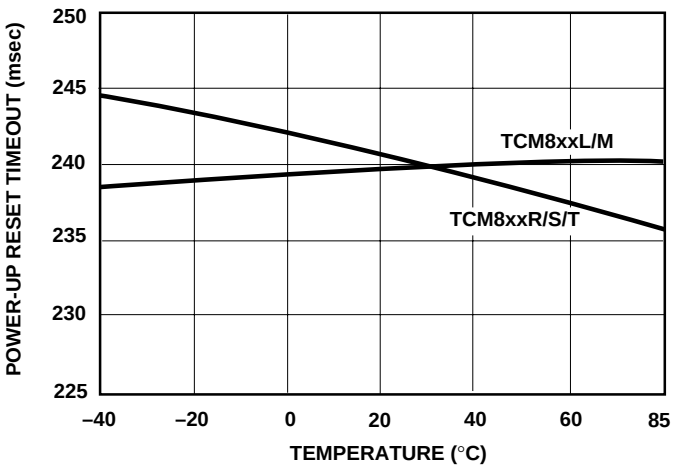
Power-Down Reset Delay vs. Temperature (TCM8xxR/S/T)



Power-Down Reset Delay vs. Temperature (TCM8xxL/M)



Power-Up Reset Timeout vs. Temperature



Normalized Reset Threshold vs. Temperature